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Final Submission README

Final Directory: The final directory is located on the virtual machine in Robert Costanzo's (rwc3bf) account. The directory with all our files is located in:

rwc3bf/cadence/ECE4332_VLSI

How to Simulate

In order to simulate and analyze our design, open in Cadence the schematic: **rwc_FinalTB_2x2** (located in the directory stated above). Then, Launch ADE L. Once open, load the state: **TestState**. Now, simply netlist and run. When the simulation is complete, we just used direct plots of the transient results. This saved test state is only the Typical-Typical, nominal VDD (1.1v), and room temperature (27°C) process. To verify process corners, we manually adjusted the state one simulation at a time (for lack of knowledge on using scripts for easier simulation).

Top Level Schematics

- **rwc_FinalIntegration**
  This is the topmost schematic for the entire cache, with the 32 blocks of SRAM, decoders, muxes, everything.
- **rwc_FinalTB_2x2**
  This is the 2 by 2 array model we used when verifying the functionality of our design. This includes a 2x2 array, model bit cells attached to represent loads, and a small version of the output MUX. The decoders used in the model are newly implemented static cmos decoders as we found problems with our original transmission gate decoders. However, the larger versions of the decoders have not been revised to the new implementation scheme.

Other Schematics of Interest

- **rwc_Final6TSRAM**
  schematic of final 6T SRAM bit cell design
- **rwc_FinalBlockDeMUX**

schematic of the DeMUX that routes the input data to the appropriate block (out of 32)

- **rwc_FinalBlockDecoder**
  schematic of the Decoder (before static cmos revision) that is ANDed with the WL decoder to drive the wordlines of a specific block only.
- **rwc_FinalColumnMUX**
  schematic of the DeMUX that routes the input data received from the block DeMUX to the appropriate BL and BLB write drivers of a block.
- **rwc_FinalDecoderInterface**
  schematic of the bank of AND gates that and the WL and Block decoders
- **rwc_FinalOutputMUX**
  schematic of MUX that selects which of the sense amps to read from and output to OUT
- **rwc_FinalSRAM_Array**
  schematic of the SRAM block. An array of 64 rows by 32 columns.
- **rwc_FinalSenseAmp**
  schematic of the sense amp used in our design and tests.
- **rwc_FinalWLDecoder**
  schematic of the decoder that selects which of 64 wordline (rows) to utilize.

Top Level Layouts

- **hls_FullChip**
  This is the topmost layout which includes the 32 blocks of SRAM and decoder. Other peripheries are not present.
- **hls_6TSRAMOpt**
  This is the main SRAM design which is DRC and LVS clean. This verifies the functionality of the 1 bit cell. It also demonstrates its ability to be easily tiled and displays rails and wells extending to the edge of the cell.

Other Layouts of Interest

- **hls_6TSRAMOpt2X2**
  layout of the bitcell 2 by 2 showing tiling capabilities
- **hls_6TSRAMOpt32X64**
  layout of an entire block of SRAM lain out 32 by 64
- **hls_Decoder32bit**
  layout of the 1 to 32 decoder used for block or column decoding(before static cmos revision)

- **hls_Decoder64bit**
  layout of the 1 to 64 decoder used to select the world line (before revisions)
- **hls_Inverter**
  layout of the inverter DRC and LVS clean
- **hls_SenseAmp**
  layout of the final sense amp used in our design and tests
- **hls_TransmissionGate**
  layout of the traditional transmission gate used in a majority of the MUX designs